UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/694,873	10/28/2003	John G. Heston	004578.1377	4101

7590 03/14/2006

T. Murray Smith, Esq.
Baker Botts L.L.P.
Suite 600
2001 Ross Avenue
Dallas, TX 75201-2980

EXAMINER	
SANDVIK, BENJAMIN P	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 03/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/694,873	HESTON, JOHN G.	
	Examiner	Art Unit	
	Ben P. Sandvik	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1-24 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5, 10-12, 15-19, 22, 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Hoffman (U.S. Patent #6576998).

With respect to **claims 1 and 15**, Hoffman teaches a circuit having first (Fig. 5, 26), second (Fig. 5, 208), and third circuit portions (Fig. 5, 36), said first circuit portion including at least one semiconductor component (Col 3 Ln 8) and said third circuit portions including a single semiconductor circuit component (Col 2 Ln 57), and said second circuit portion including at least one non-semiconductor circuit component and being free of semiconductor circuit components, said second circuit portion having first and second electrically conductive parts (Fig. 5, portions of 208 connected to third circuit portion 36), and said third circuit portion having third and fourth electrically conductive parts which are respectively coupled to said first and second electrically conductive parts (Fig. 5, 44) by respective thermo-formed bonds (Col 9 Ln 4-6); a first substrate

(Fig. 5, 12 and 26) with said first and second circuit portions disposed adjacent one side thereof, said first substrate having a semiconductor portion which has each said semiconductor circuit component of said first circuit portion therein (Fig. 5, 26); and a second substrate with said third circuit portion disposed adjacent one side thereof (Fig. 5, 36), said second substrate being physically separate from said first substrate and being oriented so that said one side thereof faces said one side of said first substrate, and said second substrate having a semiconductor portion which has said single semiconductor circuit component of said third circuit portion therein (Col 2, Ln 57) and said second substrate being devoid of any other semiconductor circuit component: and wherein the second substrate and the second circuit portion have no electrical connection therebetween other than any electrical connection formed between the first and second electrically conductive parts of the second circuit portion and the third and fourth electrically conductive parts of the third circuit portion (portion 36 has only two connection parts; the connection between parts 44 and 22 is the only electrical connection to portion 36).

With respect to **claims 2 and 16**, Hoffman teaches that said first circuit portion has one said circuit component thereof which is implemented in a first semiconductor technology, and that said third circuit portion has one said circuit component thereof which is implement in a second semiconductor technology different from said first semiconductor technology (Col 2 Ln 52-59, the first circuit

portion is a semiconductor chip and the third portion could be a laser diode, for example).

With respect to **claims 3 and 17**, Hoffman teaches that said circuit includes a fourth circuit portion which includes at least one semiconductor circuit component (Fig. 5, other device 36), said second circuit portion having fifth and sixth electrically conductive parts (portions of 208 connected to 36), and said fourth circuit portion having seventh and eight electrically conductive parts which are respectively coupled to said fifth and sixth electrically conductive parts by respective thermo-formed bonds (Fig. 5, 44); and including a third substrate with said fourth circuit portion disposed adjacent one side thereof (Fig. 5, 36), said third substrate being physically separate from said first and second substrates and being oriented so that said one side thereof faces said one side of said first substrate, and said third substrate having a semiconductor portion which has each said semiconductor circuit component of said fourth circuit portion therein (Col 2 Ln 57).

With respect to **claims 4 and 18**, Hoffman teaches that said third circuit portion has one said circuit component thereof which is implemented in a first semiconductor technology; and that said fourth circuit portion has one said circuit component thereof which is implemented in a second semiconductor technology different from said first semiconductor technology (Col 5 Ln 23-25).

With respect to **claims 5 and 19**, Hoffman teaches that said first circuit portion has one said circuit component thereof which is implemented in a third

semiconductor technology different from ach of said first and second semiconductor technologies (Col 5 Ln 23-25).

With respect to **claim 10**, Hoffman teaches that said third circuit portion has therein a single said circuit component (Col 2 Ln 57, a single transistor for example).

With respect to **claims 11 and 22**, Hoffman teaches that said single circuit component of said third circuit portion is a transistor (Col 2 Ln 57).

With respect to **claims 12 and 23**, Hoffman teaches that the first substrate is a semiconductor substrate (Col 2 Ln 52-59).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoffman, in view of Akram et al (U.S. PG Pub #2002/0125558).

With respect to **claims 6 and 20**, Hoffman does not teach that the bonds are one of a thermosonic and a thermocompression bond. Akram teaches wire bonds which are thermosonic bonds (Paragraph 6). It would have been obvious to one of ordinary skill in the art to form the bond of Hoffman using a thermosonic process as taught by Akram in order to create a strong bond to the device.

Claims 9 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoffman.

With respect to **claims 9 and 21**, Hoffman does not explicitly state that said third circuit portion has one said circuit component thereof with a fabrication yield which is lower than a fabrication yield of each said circuit component of said first circuit portion. However, Hoffman teaches that the circuit portions can be different devices (Col 2 Ln 57). It would have been obvious to one of ordinary skill in the art at the time the invention was made that the first and third circuit portions of Hoffman have different fabrication yields and to provide the circuit with lower fabrication yield as the third circuit portion in order to increase the final yield of the finished package by fabricating the circuit portions separately and joining them later.

Furthermore, with respect to **claim 9**, note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product

produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear.

As to the grounds of rejection under section 103, see MPEP § 2113

Claims 13 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoffman, in view of Hatada (U.S. Patent #4693770).

With respect to **claims 13 and 24**, Hoffman does not teach that the first substrate includes one of silicon and gallium arsenide; and that said second substrate includes gallium arsenide. Hatada teaches semiconductor substrates comprising gallium arsenide (Col 4 Ln 8-12). It would have been obvious to one of ordinary skill in the at the time the invention was made to make the semiconductor substrates of Hoffman out of gallium arsenide because it has been shown to be a suitable semiconductor material.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hoffman, in view of Sayagani et al (U.S. PG Pub #20020072147).

With respect to **claim 14**, Hoffman teaches all of the limitations of claim 1, but does not teach that the circuit is a microwave circuit. Sayagani teaches a multi-chip package that is used as a high-frequency package (Fig. 1 and Paragraph 39). It would have been obvious to one of ordinary skill in the art at

the time the invention was made to make the package of Hoffman a high-frequency package usably in microwave applications as taught by Sayagani in order to use the package as a high frequency signal processor.

Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shiraishi et al (U.S. PG Pub #2001/0002727), in view of Perino et al (U.S. Patent #6621155).

With respect to **claim 25**, Shiraishi teaches a circuit having first (Fig. 4, 105), second (Fig. 4, 101), and third circuit portions (Fig. 4, 103), said first and third circuit portions each including at least one semiconductor circuit component, said second circuit portion having first and second electrically conductive parts (Fig. 4, solder balls under 101); a first substrate with said first circuit portion disposed adjacent one side thereof (Fig. 4, substrate of chip 105), said first substrate having a semiconductor portion which has each said semiconductor circuit component of said first circuit portion therein; an insulating layer overlying the first circuit portion (Fig. 4, insulating layer of multi-layer board 107); at least one via disposed within the insulating layer and electrically coupling the first circuit portion to the second circuit portion (Fig. 4, 109); and a second substrate with said third circuit portion disposed adjacent one side thereof said second substrate being physically separate from said first substrate and being oriented so that said one side thereof faces said one side of said first substrate, and said second substrate having a semiconductor portion which has each said semiconductor circuit component of said third circuit portion therein (Fig. 4,

substrate of chip 103). Shiraishi does not teach that said second circuit portion includes at least one passive component selected from the group consisting of a resistor, a capacitor, and an inductor, and being free of semiconductor circuit components; and said third circuit portion having third and fourth electrically conductive parts which are respectively coupled to said first and second electrically conductive parts by respective thermo-formed bonds. Perino teaches a circuit portion (Fig. 9, 950) having passive components (Fig. 9, 940a-c) electrically coupled to a semiconductor die; the circuit portion having first and second conductive parts (Fig. 9, bond pads for passive components 940a, 940b) and being coupled to third and fourth conductive parts of the chip (Fig. 9, bond pads connected to passive components 940a, 940b). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the chip 103 of Shiraishi with a second circuit portion as taught by Perino in order to terminated transmission lines on the chip stack.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ben P. Sandvik whose telephone number is (571) 272-8446. The examiner can normally be reached on Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

bps